AMENDMENTS TOTHE CLAIMS

1. (Currently amended) A method for multiple memory aliasing for a configurable system-on-a-chip, the configurable system on a chip integrating at least a central processing unit (CPU), an internal system bus, a programmable input/output, and a programmable logic, on a single integrated circuit device, the method comprising:

executing code from a read-only memory (ROM) internal memory by the CPU, said ROM internal memory having an enabled alias and fetching the code from the ROM in response to the enabled alias;

searching, by the code executing from the ROM, for a valid secondary initialization routine to configure the system including system peripherals;

~~locating a configuration program in the ROM internal memory;~~

disabling the ROM internal memory alias, and disabling fetching of the code from the ROM in response to the disabled alias; [[and]]

jumping to the secondary initialization routine located in a FLASH external memory;

configuring the system-on-a-chip using the secondary initialization routine located in the FLASH external memory; and

resetting the CPU after completion of the configuring of the system-on-a-chip.

Claims 2-3. (Cancelled)

4. (Currently Amended) The method of claim 1 ~~3~~ further comprising:

executing code starting with the bottom of the FLASH external memory.

5. (Original) The method of claim 1, wherein the FLASH external memory has an external alias, the method further comprising:

selectively programming the alias of the ROM internal memory;

selectively programming the external alias of the FLASH external memory; and

programming the priority of the alias and the external alias.

6. (Currently Amended) An apparatus for multiple memory aliasing for a configurable system-on-a-chip, the configurable system on a chip integrating at least a central processing unit, an internal system bus, a programmable intput/output and a programmable logic, on a single integrated circuit device, ~~the method~~ comprising:

means for executing code from an internal memory by the CPU, said internal memory having an enabled alias, and fetching the code from the ROM in response to the enabled alias;

means for searching for a valid secondary initialization routine to configure the system including system peripherals;

~~means for locating a configuration program in the internal memory;~~

means for disabling the internal memory alias; [[and]]

means for jumping to the secondary initialization routine;

means for configuring the system-on-a-chip using the secondary initialization routine; and

means for resetting a central processing unit of the system-on-a-chip.

Claims 7-8. (Cancelled)

9. (Currently amended) The apparatus of claim 6 [[8]] further comprising:

means for executing code starting with the bottom of the external memory.

10. (Original) The apparatus of claim 9 further comprising:

mans for setting up an application program for the system-on-a-chip from the internal memory.

11. (Currently amended) A computer readable medium having instructions which, when executed by a processing system, cause the system to perform a method for multiple memory aliasing for a configurable system-on-a-chip, the configurable system on a chip integrating at least a central processing unity, an internal system bus, a programmable input/output, and a programmable logic, on a single integrated circuit device, the method comprising:

executing code from an internal memory by the CPU, said internal memory having an enabled alias, and fetching the code from the ROM in response to the enabled alias;

searching, by the code executing from the ROM, for a valid secondary initialization routine to configure the system including system peripherals;

~~locating a configuration program in the internal memory;~~

disabling the internal memory alias; [[and]]

jumping to the secondary initialization routine;

configure the system-on-a-chip using the secondary initialization routine; and

reset a central processing unit of the system-on-a-chip.

Claims 12-13. (Cancelled)

14. (Currently amended) The medium of claim 11 [[13]], wherein the executed instructions further cause the system to:

execute code starting with the bottom of the external memory.

15. (Original) The medium of claim 14, wherein the executed instructions further cause the system to:

set up an application program for the system-on-a-chip from the internal memory.

16. (New) A method for configuring a system-on-a-chip, comprising:

commencing execution of a primary initialization routine at a base address of address space mapped to a ROM in the system-on-a-chip by a processor in the system-on-a-chip;

transferring control, in response to a control transfer instruction executed by the processor, to a secondary initialization routine in address space to a memory device external to the system-on-a-chip, and fetching and executing code from the external memory device by the processor;

programming configurable logic resources on the system-on-a-chip by execution of the secondary initialization routine; and

remapping the base address to the external memory device in response to completion of the secondary initialization routine; and

commencing execution by the processor of code at the base address remapped to the external memory device.

17. (New) The method of claim 16, further comprising

resetting the processor a first time;

wherein the commencing execution of the primary initialization routine is in response to the first resetting of the processor;

resetting the processor a second time after the programming of the configurable logic resources and the remapping of the base address to the external memory.

18. (New) The method of claim 17, further comprising mapping the base address to the ROM in response to the first resetting of the processor.

19. (New) The method of claim 18, wherein the second resetting of the processor is performed by the secondary initialization routine.

20. (New) The method of claim 17, wherein the first resetting of the processor is in response to powering on the system-on-a-chip.

21. (New) The method of claim 16, further comprising executing by the processor a real-time operating system stored in the external memory beginning at the base address.

22. (New) An apparatus for configuring a system-on-a-chip, comprising:

means for commencing execution of a primary initialization routine at a base address of address space mapped to a ROM in the system-on-a-chip by a processor

in the system-on-a-chip;

means for transferring control, in response to a control transfer instruction executed by the processor, to a secondary initialization routine in address space to a memory device external to the system-on-a-chip, and fetching and executing code from the external memory device by the processor;

means for programming configurable logic resources on the system-on-a-chip by execution of the secondary initialization routine; and

means for remapping the base address to the external memory device in response to completion of the secondary initialization routine; and

means for commencing execution by the processor of code at the base address remapped to the external memory device.